1. For the single cycle processor design shown in the lecture slide 23 of wk2_1, assume
   - register/memory set-up times are 0.5 ns,
   - the propagation delay (clock-to-Q) of a flip-flop (register) is 0.5 ns,
   - the memory access delay time is 5 ns,
   - the delay of the control path (decoder) is 0.5 ns,
   - the register file access delay is 1 ns,
   - the delay of a MUX is 0.5 ns,
   - the delay of a zero or sign extender is 0.1 ns,
   - the delay of ALU is 2 ns, and
   - the delay of an adder is 1.5 ns,

   It is also assumed that the register/memory hold times are relatively very small and can be ignored. What is the minimum clock cycle time?

2. Refer to the slide P5 of wk2_1.
   a. What is the logic expression for control signal RegWr?
   b. How is signal Equal generated?

3. Implement the pseudo instruction (accepted by the MIPS assembler): \textit{abs} $t2$, $t3$, with a minimum number of MIPS core instructions. The \textit{abs} instruction gets the absolute value of a 2's complement integer, namely, register $t2$ has a copy of register $t3$ if the value is positive, or the two's complement of the value if it is negative.

4. P&H (1.5) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
   a. Which processor has the highest performance expressed in instructions per second?
   b. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

5. P&H (1.6) Consider two different implementations (P1 and P2) of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (Class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
   Given a program with an instruction count of $1.0E6$ instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
   a. What is the global CPI for each implementation?
   b. Find the clock cycles required in both cases.